CLAIMS:

1. A method of forming a floating gate transistor, comprising:

providing a substrate comprising semiconductive material;

forming a first layer over the semiconductive material;

forming at least one pair of spaced shallow trench isolation (STI) structures extending through the first layer and extending into the semiconductive material;

removing at least a portion of the first layer between the spaced STI structures effective to form a recess there between;

forming a conductive floating gate material to at least partially fill the recess; and

forming a control gate operatively over the conductive floating gate material.

2. The method of Claim 1, where the STI structures comprise a high density plasma (HDP) deposited oxide material.

3. The method of Claim 1, where the removing at least a portion of the first layer comprises removing substantially all of the first layer between the spaced STI structures.

4. The method of Claim 1, where the floating gate conductive material comprises a polycrystalline silicon material.

5. The method of Claim 1, further comprising forming a gate dielectric layer within the recess prior to forming the conductive floating gate material.

6. The method of Claim 1, where the conductive floating gate material completely fills the recess.

7. The method of Claim 6, where forming the conductive floating gate material comprises roughening an outermost surface of the conductive floating gate material from what it was prior to the roughening.

8. The method of Claim 7, where the roughening comprises chemical etching.

9. The method of Claim 7, where the roughening comprises forming a rugged conductive material layer on the conductive floating gate material.

10. The method of Claim 1, where the forming of the control gate comprises first forming a dielectric layer over the conductive floating gate material.

11. A method of forming a floating gate transistor, comprising:

providing a substrate comprising semiconductive material;

forming a pair of spaced shallow trench isolation (STI) masses received within and projecting outwardly from the semiconductive material, the masses defining a recess therebetween over the semiconductive material, the masses having opposing sides facing the recess;

removing material from the opposing sides effective to widen at least a portion of the recess;

forming conductive floating gate material within the widened recess effective to extend completely across the widened recess in at least one cross section; and

forming a control gate operatively over the conductive floating gate material.

12. The method of Claim 11, where the STI masses comprise a high density plasma (HDP) deposited oxide material.

13. The method of Claim 12, where the STI masses comprise tops elevationally above the opposing sides and where removing material from opposing sides further comprises removing material from the tops at a rate slower than the material removal rate from the sides.

14. The method of Claim 11, where the STI masses further define an active area within the semiconductor material and comprise tops elevationally above the opposing sides; where the portion of the widened recess has a first cross section dimension proximate the tops and the active area has a smaller, second cross section dimension parallel with the first cross section dimension and proximate an uppermost surface of the semiconductive material.

15. The method of Claim 11, where the pair of spaced STI masses are substantially parallel and spaced from one another.

16. The method of Claim 11, where:

the STI masses have tops; and

prior to forming the control gate, planarizing uppermost conductive floating gate regions of the conductive floating gate material.

17. The method of Claim 16, where the planarizing comprises chemical mechanical polishing.

18. The method of Claim 11, where the conductive floating gate material comprises a polycrystalline silicon material.

19. The method of Claim 11, further comprising forming a gate dielectric layer within the recess prior to forming the conductive floating gate material.

20. The method of Claim 11, where the conductive floating gate material only partially fills the recess.

21. The method of Claim 6, where forming the conductive floating gate material comprises roughening an outermost surface of the conductive floating gate material from what it was prior to the roughening.

22. A method of forming a floating gate transistor, comprising:

providing a substrate comprising semiconductive material;

forming a pair of spaced shallow trench isolation (STI) masses received within and projecting outwardly from the semiconductive material, the masses defining a recess there between over the semiconductive material;

forming conductive floating gate material within the recess effective to extend completely thereacross in at least one cross section, the conductive floating gate material comprising an outermost surface;

chemically etching the outermost surface effective to increase its roughness and surface area from what it was prior to the chemical etching; and

after the chemical etching, forming a control gate operatively over the floating gate conductive material.

23. The method of Claim 22, where the pair of STI masses comprise a high density plasma (HDP) deposited oxide material.

24. The method of Claim 22, where the pair of STI masses have opposing sides facing the recess and further comprising removing material from the opposing sides effective to widen at least a portion of the recess.

25. The method of Claim 24, where the pair of STI masses have tops elevationally above the sides and further comprising removing material from the tops at a rate slower than the material removal rate from the sides.

26. The method of Claim 24, where the STI masses further define an active area within the semiconductor material and comprise tops elevationally above the opposing sides; where the portion of the widened recess has a first cross section dimension proximate the tops and the active area has a smaller, second cross section dimension parallel with the first cross section dimension and proximate an uppermost surface of the semiconductive material.

27. The method of Claim 22, where the pair of spaced STI masses are substantially parallel and spaced from one another.

28. The method of Claim 22, where:

the STI masses have tops; and

prior to forming the control gate, planarizing uppermost conductive floating gate regions of the conductive floating gate material.

29. The method of Claim 28, where the planarizing comprises chemical mechanical polishing.

30. The method of Claim 22, where the conductive floating gate material comprises a polycrystalline silicon material.

31. The method of Claim 22, further comprising forming a gate dielectric layer within the recess prior to forming the conductive floating gate material.

32. The method of Claim 22, where the conductive floating gate material only partially fills the recess.

33. The method of Claim 22, where the conductive floating gate material comprises an essentially concave uppermost surface.

34. The method of Claim 22, where forming the conductive floating gate material comprises roughening an outermost surface of the conductive floating gate material from what it was prior to the roughening.

35. The method of Claim 34, where the roughening comprises chemical etching.

36. The method of Claim 34, where the roughening comprises forming a rugged conductive material layer on the conductive floating gate material.

37. The method of Claim 22, further comprising forming a dielectric layer over the conductive floating gate material prior to forming the control gate.

38. A method of forming a floating gate transistor, comprising:

providing a substrate comprising semiconductive material;

forming a patterned masking material over the semiconductive material, the masking material being patterned for defining isolation trenches within the semiconductive material;

using the patterned masking material as a mask, removing semiconductive material from the substrate effective to at least partially form at least two shallow isolation trenches within the semiconductive material and semiconductive active area between the at least two trenches;

after the removing of the semiconductive material, forming insulative isolation material within the at least two trenches and which projects outwardly from the semiconductive material;

after forming the insulative isolation material, removing at least a portion of the masking material effective to define a recess between two shallow trench isolation masses comprising the insulative isolation material which project outwardly from the semiconductive material;

forming a conductive floating gate material to at least partially fill the recess; and

forming a control gate operatively over the floating gate conductive material.

39. The method of Claim 38, where the insulative isolation material comprises a high density plasma (HDP) deposited oxide material.

40. The method of Claim 38, where the removing at least a portion of the masking material comprises removing substantially all of the masking material from between the two shallow trench isolation masses.

41. The method of Claim 38, where the removing at least a portion of the masking material comprises:

removing substantially all of the masking material from between the two shallow trench isolation masses;

the outwardly projecting insulative isolation material having sides facing the recess; and

removing portions of the sides effective to widen the recess.

42. The method of Claim 41, where the outwardly projecting insulative isolation material has tops elevationally above the sides and the removing portions of the sides comprises etching the tops and the sides of the outwardly projecting insulative isolation material, the sides etching at a greater rate than the tops.

43. The method of Claim 38, where two of the at least two trenches are substantially parallel and spaced from one another effective for defining a semiconductor active area therebetween.

44. The method of Claim 38, where the conductive floating gate material completely fills the recess.

45. The method of Claim 38, where forming the conductive floating gate material comprises roughening an outermost surface of the conductive floating gate material from what it was prior to the roughening.

46. The method of Claim 45, where the roughening comprises chemical etching.

47. The method of Claim 45, where the roughening comprises forming a rugged conductive material layer on the conductive floating gate material.

48. The method of Claim 47, where the rugged conductive material layer comprises hemispherical grain polysilicon.

49. A floating gate transistor structure, comprising:

a substrate comprising semiconductive material;

a pair of spaced shallow trench isolation (STI) masses received within and projecting outwardly from the semiconductive material, the masses having opposing sides defining a region therebetween over the semiconductive material and an active area therebetween within the semiconductive material;

a floating gate received within the region and over the active area; and

a control gate operatively over the floating gate.

50. The floating gate transistor of Claim 49, where the floating gate only partially fills the region.

51. The floating gate transistor of Claim 49, where the floating gate completely fills the region.

52. The floating gate transistor of Claim 49, where the floating gate comprises a roughened uppermost surface.

53. The floating gate transistor of Claim 49, where the floating gate only partially fills the region and comprises an essentially concave uppermost surface.

54. The floating gate transistor of Claim 49, where the floating gate comprises hemispherical grain polysilicon.

55. The floating gate transistor of Claim 49, where the active area has a first cross-sectional dimension and the region has a second cross-sectional dimension, the first cross-sectional dimension being parallel to and smaller than to the second cross-sectional dimension.

56. The floating gate transistor of Claim 55, where the floating gate only partially fills the region and comprises an essentially concave uppermost surface.

57. The floating gate transistor of Claim 55, where the floating gate comprises a roughened uppermost surface.

58. The floating gate transistor of Claim 49, where the active area has a first cross-sectional dimension and the region has a second cross-sectional dimension, the first cross-sectional dimension being parallel to and essentially equal to the second cross-sectional dimension.

59. The floating gate transistor of Claim 58, where the floating gate only partially fills the region and comprises an essentially concave uppermost surface.

60. The floating gate transistor of Claim 59, where the essentially concave uppermost surface is roughened.

61. A floating gate transistor structure, comprising:

a substrate comprising semiconductive material;

a pair of spaced shallow trench isolation (STI) masses having first portions received within the semiconductive material and second portions projecting outwardly from the semiconductive material, the first and second portions each having opposing sides, the opposing sides of the first portions defining an active area therebetween having a first cross-sectional dimension and the opposing sides of the second portions defining a region therebetween having a second cross-sectional dimension;

a first dielectric layer received within the region and overlying the active area;

a floating gate received within the region and overlying the gate oxide layer;

a second dielectric layer overlying the floating gate; and

a control gate operatively overlying the second dielectric layer and operatively coupled to the floating gate.

62. The floating gate transistor of Claim 61, where the second cross-sectional dimension is larger than the first cross-sectional dimension.

63. The floating gate transistor of Claim 61, where the floating gate only partially fills the region and comprises an essentially concave uppermost surface.

64. The floating gate transistor of Claim 63, where the floating gate comprises hemispherical grain polysilicon.

65. The floating gate transistor of Claim 61, where the floating gate completely fills the region and comprises a rugged outermost surface.

66. The floating gate transistor of Claim 61, where the second cross-sectional dimension is essentially equal to the first cross-sectional dimension.

67. The floating gate transistor of Claim 66, where the floating gate comprises hemispherical grain polysilicon, only partially fills the region and has an essentially concave uppermost surface.

68. The floating gate transistor of Claim 66, where the floating gate completely fills the region.

69. The floating gate transistor of Claim 68, where the floating gate comprises a rugged outermost surface.